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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,797	08/29/2003	Toshifumi Iwasaki	242006US2	7464

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EXAMINER	
LUU, CUONG V	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,797	IWASAKI, TOSHIFUMI	
	Examiner	Art Unit	
	Cuong V. Luu	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☒ Claim(s) *2-4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-4 are pending. Claims 1-4 have been examined. Claims 2-4 have been objected.

Claim 1 has been rejected.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-4 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

1. As per claim 1, the Examiner respectfully submits, under current PTO practice, that the claimed invention does not recite a tangible result and is merely drawn to a manipulation of abstract ideas. The claims are not tangible because the results of the final step of the method is not used in such a way to make them tangible such as displaying to users or storing for later usage.

2. Claims 2-4 inherit the defects of claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Scott et al, herein Scott, (NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress, IEEE 1999. Since the 4 pages in this paper are not numbered, the Examiner numbers them from 1 to 4 starting with the 1st page).

1. As per claim 1, Scott teaches a method of designing a semiconductor device, said semiconductor device to be designed comprising:

a semiconductor substrate (p. 1, col. 1 of the page, Introduction section, paragraph 1 of the section. The teaching of layout of CMOS device inherits this limitation);

an element isolation insulating film provided in a part of a main surface of said semiconductor substrate (p. 1, col. 1 of the page, Introduction section, paragraph 1 of the section. The teaching of layout of CMOS device inherits this limitation);

a gate structure provided on a part of said main surface of said semiconductor substrate, said gate structure being placed in an element forming region defined by said element isolation insulating film (p. 1, col. 1 of the page, Introduction section, paragraph 1 of the section. The teaching of layout of CMOS device inherits this limitation); and

source/drain regions provided in said main surface of said semiconductor substrate in said element forming region, said source/drain regions forming a pair holding a channel forming region defined under said gate structure therebetween (p. 1, col. 1 of the page, Introduction section, paragraph 1 of the section. The teaching of layout of CMOS device inherits this limitation), wherein

stress exerted on an area of said semiconductor substrate is controlled depending on a shape of said element forming region, said area of said semiconductor substrate holding said gate structure thereover (p. 1, col. 1 of the page, Abstract section. The teaching of stress varies with distance from the trench edge implies that the shape affects the stress exerted on an area).

Allowable Subject Matter

Claims 2-4 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 101, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

2. As per claim 2, the prior art does not teach said element forming region includes in top view at least one projecting portion provided along a perimeter of said element forming region as recited by the claimed invention.

3. As per claim 3, the prior art does not teach said element forming region includes in top view at least one recessed portion provided along a perimeter of said element forming region.

4. As per claim 4, the prior art does not teach in top view, a corner of said element forming region is greater in curvature than a corner of an element-forming region defined by an element isolation insulating film, which is formed by a patterning process using a photomask having a rectangular opening pattern.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong V. Luu whose telephone number is 571-272-8572. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah, can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. An inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CVL

KAMINI SHAH
SUPERVISORY PATENT EXAMINER